REMARKS

Entry of this response is proper under 37 CFR §1.116, since there are no new claims, claim amendments, or new issues raised herein.

Claims 1-4, 6, 10-15, and 23-30 are all the claims presently pending in the application. Claims 5, 7-9, and 16-22 are canceled.

It is noted that Applicants specifically state that no amendment to any claim herein, if any, should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-4, 6, 10-15, and 23-30 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over US Patent Publication 2004/0173812 to Currie, et al., further in view of US Patent Publication 2004/0108559 to Sugii, et al., US Patent Publication 2005/0242395 to Chen et al.

Applicants again traverse this rejection, as revised, in the discussion that follows.

I. THE CLAIMED INVENTION

As described and defined in, for example, claim 1, the present invention is directed to a method of forming a FinFET (Fin Field Effect Transistor) containing a plurality of fins interconnected by fin connectors. At least one localized stressor region is formed within the device, the at least one localized stressor region being located on one of the fin connectors as a region of stressor material filling in an interior portion of the fin connector.

Conventional methods, such as described in paragraphs [0005] through [0007], strain FinFETs by Si or SiGe, but have caused defects, thereby lowering yields.

The claimed invention, on the other hand, provides a localized stressor embedded within the device.

II. THE PRIOR ART REJECTION

In summary, Applicants again respectfully submit that the prior art rejection of record

fails to demonstrate all elements of the claimed invention, since there is no demonstration of providing a localized stressor on the fin connectors of a finFET as a filled-in region on the interior portion of the finFET fin connectors.

Applicants are unable to find any reasonable support in either previously-cited Currie or previously-cited Sugii or newly-cited Chen, to form a localized stressor within the interior region of a fin connector of a FinFET, as required by the plain meaning of the claim language. The most that can reasonably be deduced from the references of record is that FinFETs were known in the art at the time of the invention and that the claimed invention, therefore, would have been possible. Indeed, on page 7 of the latest Office Action, the Examiner clearly states that the standard being applied in the present evaluation is based on the conclusion that one of skill "would have recognized" that the claimed invention was possible:

"*It would have been obvious to one having ordinary skill in the art at the time the invention was made to have recognized that localized stressor trench (recess) region can be formed on a fin connector as shown in fig. 28 of Sugii et al. or figs. 3-5 of Chen et al. because [a] fin connector connects source/drain regions of two FET transistors together*."

However, such demonstration is insufficient, since the correct standard for obviousness requires an articulation of a reasonable rationale to modify the primary reference to arrive at the claimed invention, and the rejection of record is based on the wrong standard for obviousness. A mere conclusory statement that one of skill would have "recognized that the claimed invention was possible at the time of the invention" is nothing but a rationale based on improper hindsight.

That is, the Examiner makes no attempt to demonstrate that the differences between primary reference Currie and the claimed invention were obvious because the differences were known in the art as being either a substitute or an improvement (or any of the other five rationales mentioned in *KSR*). Indeed, since the rejection of record fails even to demonstrate any suggestion of localized stressing except a source/drain and fails to demonstrate any objective suggestion that one of skill would use a fin connector, rather than the source/drain, it must be concluded that the only source of the suggestion for such modification derives from the disclosure of the present invention, thereby supporting the legal conclusion that the claimed invention is clearly non-obvious.

In the rejection of record and as best understood for the rejection described on page 2 of

the Office Action, the Examiner seems to consider that regions 144, 148 shown in Figures 10D/10E of primary reference Currie, either to be localized stressor regions or to be fin connector or to be localized stressor regions on fin connectors. Alternatively, at the top of page 3, the Examiner seems to consider that primary reference Currie satisfies the description of the claimed invention because the Examiner is able to consider that the underlying gate structure component 18 can be considered to be a fin of a finFET. As best understood, the Examiner relies upon secondary references Chen and Sugii as evidence that finFET were known in the art.

Applicants respectfully submit that the rejection of record fails to establish a *prima facie* obviousness rejection supporting any of the seven rationales mentioned in *KSR*.

Applicants begin by pointing out that the independent claims clearly refer to localized stressor regions formed on the interior portion of the fin connector of a finFET device. Primary reference Currie fails to satisfy the plain meaning of the claim language of even the independent claims, since "finFET" and "fin connector" are terms of art that Applicants understand the Examiner intends to demonstrate in the secondary references.

Contrary to the Examiner's allegation, regions 144, 148 of Figure 10D are source/drain regions, not fins, and the embodiment shown in Figures 10D/10E is showing the partial removal of the source/drain and subsequent deposit of material 150 having lattice constant larger than that of Si, as clearly described beginning at paragraph [0077]. However, to one having ordinary skill in the art, the source/drain of an FET is not equivalent to a fin connector of the claimed invention. Nor do the regions 144, 148 even correspond to an interior region of the source/drain, let alone an interior region of a fin connector, as required by the independent claims.

Relative to region 18, which the Examiner at the top of page 3 refers to as a "fin", Applicants point out that, to one having ordinary skill in the art, structure 18 in Figure 10D is merely the lower layer of sidewall spacer structures 120, 122 (see final sentence of paragraph [0065]), with structure 18 being the layer of the spacer structure formed by strained layer 18. To one having ordinary skill in the art, a gate sidewall structure is not equivalent to a fin connector of a finFET.

The Examiner makes no attempt to identify the differences between the claimed invention and the configurations shown in Currie, from the perspective of one of ordinary skill in the art, let alone attempt to articulate a reasonable rationale to modify Currie to satisfy the

claimed invention. Therefore, the rejection of record fails to establish a *prima facie* obviousness rejection.

Hence, turning to the clear language of the claims, in Currie, even if modified by Sugii, there is no teaching or suggestion of "... forming at least one localized stressor region within said device, said at least one localized stressor region being located on one of said fin connectors as a region of stressor material filling in an interior portion of said fin connector", as required by independent claim 1. Independent claim 14 has similar language.

For this reason alone, all claims are clearly patentable over Currie, and the Examiner is respectfully requested to reconsider and withdraw this rejection.

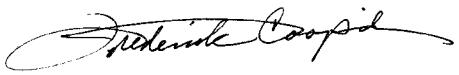
III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-4, 6, 10-15, and 23-30, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,



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